Instruction Level Profiling in ETISS Simulator

The ETISS Simulator can be used for simulating programs compiled for a variety of targets on an instruction level. The goal of the work is to make performance analysis (profiling) possible with ETISS on several abstraction levels.

Task Description:

- Survey state-of-the-art profiling methods for embedded SW
- Get used to existing set of tools (ETISS, Tracer, RISC-V SW Compiler)
- Generate Instruction Traces of Program Execution with ETISS (already implemented)
- Analyse Trace to count how often specific parts of code are executed on several levels: Instruction, "Basic Block", (For ML workloads: per Layer)
- Visualize Profiling Results
- Convert trace or profiling result to be compatible with existing (GUI-based) profiling tools

Prerequisites

- Knowledge of C++ programming language
- Preferably experience with Python Scripting
- Experience with Embedded SW Development (e.g. ARM/RISC-V)

Contact

philipp.van-kempen@tum.de

Advisors

Philipp van Kempen