Electronic Design Automation
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Seminar

Leakage Models for High-Level Power Estimation

Abstract - Leakage currents are one major concern when designing recent CMOS devices, making design for leakage at all stages of the design process mandatory. Early leakage optimization requires early leakage prediction, and for electronic system level design, this means estimation capabilities at register transfer (RT) level or above. Existing models are very accurate, but slow [transistor level such as Berkeley Simulator (BSIM)], or the slightly faster gate level models (such as the Liberty library), disregard relevant parameters.

RT level leakage macro models are presented, which are faster than recent gate level models, while preserving the accuracy of the transistor level models to a great extent. An estimation framework is proposed, describing the subthreshold, gate, and junction leakage of recent technology devices. The models are characterized using BSIM compact models and a Monte Carlo process variation description. Each varying BSIM parameter can be described. As an example of use, channel length, oxide thickness, and channel doping are regarded together with the temperature, supply voltage and body voltage. The final macro model needs less than a hundred parameters to capture the leakage behavior of an entire RT component and is still analytically describing the dependence to the process parameters. Compared to SPICE + BSIM, a model prediction is computed up to a hundred times faster for large RT components, and is, depending on the analyzed technology, within 2.1% (for 16-nm LP)-6.8% (for 65-nm bulk) deviation over a wide range of operating conditions and process variation settings.

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