Electronic Design Automation
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Forschungspraxis, Bachelor's Thesis

Dataset Generation for Graph Attention Network-based Power Estimation

In System on Chip (SoC) design, power consumption gets increasingly important (e.g. due to increasing complexity of the devices and contrary, due to the growing number of mobile applications). Although precise gate-level simulation methods exist, they are often not feasible for larger designs. Therefore, less accurate, but faster methods have been developed [1]. For dynamic power dissipation, the switching activity of a design is crucial (beside technological parameters). Here, already approaches for its estimation based on Machine Learning, namely Graph Neural Networks (GNN), have been developed [2].

But, existing approaches require detailed information about the structure of a circuit (e.g. the gate level netlist) for exact power estimation. This information may not be always available (e.g. in early design stages or in black-box IP blocks). Therefore, approaches to achieve a exact power estimation with limited knowledge would be appreciated. In previous work, a framework for power estimation based on Graph Attention Neural Networks (GAT) has been developed to obtain power estimations based on only the primary input and output signals of a design and its relationships, modelled as graphs.

In this project, a dataset with multiple reference designs (e.g. benchmark circuits or open-source cores) should be generated to enable further training of the GAT-based power estimation framework. This includes the selection of appropriate reference designs, their synthesis and physical design in respective tools and the extraction power wavefroms from gate level simulation. Furthermore, a framework for automatic dataset generation may be developed.

[1] NAJM, Farid N.; XAKELLIS, Michael G. Statistical Estimation of the, Switching Activity in VLSI Circuits. VLSI Design, 1998, 7. Jg., Nr. 3, S. 243-254.

[2] ZHANG, Yanqing; REN, Haoxing; KHAILANY, Brucek. GRANNITE: Graph neural network inference for transferable power estimation. In: 2020 57th ACM/IEEE Design Automation Conference (DAC). IEEE, 2020. S. 1-6.

Prerequisites

- Experience in Python programming would be beneficial
- Knowledge in HDLs and CMOS power consumption
- Interest in the ASIC Development Flow and Machine Learning in EDA
- Ability to work independently

Contact

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Advisors

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