Electronic Design Automation
TUM Department of Electrical and Computer Engineering
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Forschungspraxis, Master's Thesis

# Automatic Generation of RISC-V Special Instructions in SW Toolchains

RISC-V is a new, open instruction set architecture (ISA) that, as a core feature, can be extended with special instructions to customize embedded processors to special applications such as frm the control and machine learning domain.

We already developed a customizable simulator named ETISS, that can quickly evaluate the benefit of special instructions for a given application. Next to the core, also the compiler and assembler support for creating a binary from embedded C code is required by designers to exploit performance benefits of special instructions.

In this thesis, a method and implementation should be developed in order to automatically generate patches for the LLVM and GCC toochain from a formal definition of a special instruction. There are various levels of special instruction support possible in the toolchain, that should be explored within this thesis.

## Advisors

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