Master's Thesis

Extending a RISC-V RTL Fault Injection Simulation to link Architectural Error Models with Micro-Architectural Faults

Error models, such as instruction skips, instruction modifications, or register file corruptions are common methods to evaluate fault response of systems on Instruction Set Architecture (ISA) level. However, faults in instruction data or ISA registers in their respective memory are only a subset of possbile reasons that may result in such error models on ISA level. Analyzing a core w.r.t. fault injection on Register Transfer Level (RTL) considers a core's micro-architecture, where certain faults will still result in the aforementioned errors.

Prerequisites

- Advanced C++ skills
- Experience with a hardware description language (Verilog, VHDL, Chisel)
- Understanding of processor micro-architecture
- One assembly language, preferably RISC-V
- Linux CLI

Advisors

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