Scalable System Authentication on a RISC-V Platform

Nowadays embedded systems perform a broad array of tasks, while staying hidden to the user. In modern applications, such as telecommunication or automotive ones, these are not only based around a single or few microcontrollers, but a mesh of densely integrated and specialized subsystems, relying on real-time communication between each other.

With scaling system sizes and their complexity, keeping high safety and security standards is a critical challenge, especially when dealing with diverse subsystems. Granting the integrity and authenticity of the compound system is one of the prerequisites to provide trust to the user or corresponding authority. Elementary concepts from file sharing, as well as blockchain applications shall be combined to provide efficient and scalable means of authentication.

You will have the opportunity to contribute to a state-of-the-art RISC-V based hardware platform and support us in our research by developing a hardware/software co-design driven accelerator. After analyzing relevant concept parts of blockchain and hash tree implementations, accelerator design in an HDL language, as well as the software counterpart for the RISC-V core follows. In the end, the reliable authentication of subcomponents and the system as a whole will be possible.

If there are any questions regarding the topic itself or the prerequisites, please do not hesitate to contact me.

Prerequisites

* Initial experience in VHDL, Verilog or SystemVerilog
* Initial experience in simulating HDL designs
* Basic knowledge of C

Advisors

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