HDL Leakage Simulation Evaluation

Within the scope of this work, simulated leakage [1] is to be compared with leakage measured with an oscilloscope. AES has been selected as a possible target for this work, therefore a DPA on simulated traces and real traces will be performed and compared.

(This work can not be conducted remote only, as it is required to take measurements)

The information on this topic is intentionally brief, as it is an ongoing project.

[1] https://gitlab.lrz.de/tueisec/tofu

Prerequisites

- Python
- VHDL/Verilog (preferred)
- Lattice FPGAs (open source flow)

Advisors

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